

**REMARKS/ARGUMENTS**

1. In the above referenced Office Action, the Examiner rejected claims 1, 4-16, 19, and 20 under 35 USC § 103 (a) as being unpatentable over Woo (U.S. Patent No. 6,445,039) in view of Yue (U.S. Patent No. 6,597,227) and Tsuji (U.S. Patent No. 5,901,023); and claims 2, 3, 17, and 18 under 35 USC § 103 (a) as being unpatentable over Woo (U.S. Patent No. 6,445,039) in view of Yue (U.S. Patent No. 6,597,227), Kluge (U.S. Patent Application No. 2003/183403) and Tsuji (U.S. Patent No. 5,901,023). The rejection has been traversed and, as such, the applicant respectfully requests reconsideration of the allowability of claims 1-20.

2. Claims 1, 4-16, 19, and 20 have been rejected under 35 USC § 103 (a) as being unpatentable over Woo (U.S. Patent No. 6,445,039) in view of Yue (U.S. Patent No. 6,597,227) and Tsuji (U.S. Patent No. 5,901,023). The applicant respectfully disagrees with this rejection and the reasoning thereof.

Woo teaches an RFIC that, as shown in Figure 61 includes a pad ring bus structure 6002 and 6004, separate circuit blocks having separate power domains 6102, 6104, and 6106, and ESD devices 6108 coupling the separate power domains to the pad ring bus.

Yue teaches placing an inductor in series with an ESD circuit 40 to produce an ESD protector. (Column 3, lines 50-51) The inductor is effectively acting like a switch to couple the ESD circuit for low frequency signals (e.g., ESD pulses) and to disconnect the ESD circuit 40 for higher frequency signals to effectively eliminate the capacitive load of the ESD circuit 40. (Column 3, line 67, through Column 4, line 11)

Tsuji teaches placing a first protection circuit 22 for an internal circuit that is coupled to an analog power supply 12, digital power supply line 18, and a digital ground 19; and a second protection circuit 23 for an internal circuit that is coupled to an analog ground 13, the digital power supply line 18, and the digital ground line 19. As such, each

protection circuit is coupled to an analog node (e.g., analog power supply or analog ground), the digital power supply line and the digital ground line.

The combined teachings of Woo, Yue, and Tsuji do not suggest an RFIC having a first inductor assembly operably coupling the analog receive ground connection to the digital ground connection and a second inductor assembly operably coupling the analog transmit ground connection to the digital ground connection. In particular, the inductor of Yue is used as a switch to switch the ESD circuit “in” for low frequency signals (e.g., ESD pulses) and “out” for high frequency signals. The inductor is not an ESD circuit and cannot, in itself, be used as a substitute for the ESD protection circuits of Tsuji as the Examiner has suggested.

An inductor in series with an ESD circuit, as taught by Yue, is not the equivalent as the first and second inductor assemblies of the present claims. Thus, the inductor in series with the ESD circuit substituted for the ESD protection circuits of Tsuji does not render the present claims obvious.

Based on the foregoing, the applicant believes that the present rejection has been overcome.

3. Claims 2, 3, 17, and 18 have been rejected under 35 USC § 103 (a) as being unpatentable over Woo (U.S. Patent No. 6,445,039) in view of Yue (U.S. Patent No. 6,597,227), Kluge (U.S. Patent Application No. 2003/183403) and Tsuji (U.S. Patent No. 5,901,023). The applicant respectfully disagrees with this rejection and the reasoning thereof.

The applicant believes that the above arguments are applicable in distinguishing claims 2, 3, 17, and 18 over the present rejection.

For the foregoing reasons, the applicant believes that claims 1-20 are in condition for allowance and respectfully request that they be passed to allowance.

The Examiner is invited to contact the undersigned by telephone or facsimile if the Examiner believes that such a communication would advance the prosecution of the present invention.

RESPECTFULLY SUBMITTED,

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37 C.F.R. 1.8

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